CLAIMS:-

1. **A method of forming a pattern on or in a substrate surface** comprising or including the steps of:
   a) Providing a substrate;
   b) modifying the substrate surface to provide a topographical feature, or identifying a topographical feature on the substrate surface;
   c) preparing a plurality of particles;
   d) deposition of a plurality of the particles on the substrate surface in, or in the general vicinity of, the topographical feature;
   e) formation of an arrangement of particles via accumulation (by one means or another), of the particles, into or against or proximal to, the topographical feature;
   f) removing at least a portion of the substrate by etching, the arrangement of particles acting as an etch mask.

2. A method as claimed in claim 1 wherein the substrate is at least partially an insulating or semiconducting material.

3. A method as claimed in any one of the preceding claims wherein the pattern is in the form of a wire; the arrangement of particles being a substantially continuous chain of metallic clusters.

4. A method as claimed in claim 3 wherein the wire is a nanowire and the particles are nanoparticles.

5. A method as claimed in any one or more of the preceding claims wherein the modification includes formation of a step, depression or ridge in the substrate surface.

6. A method as claimed in claim 5 wherein the modification comprises formation of a groove having a substantially v-shaped cross-section or inverted pyramid structure running substantially between the contacts.

7. A method as claimed in claim 6 wherein the surface modification involves lithography.

8. A method as claimed in claim 7 wherein the surface modification step involves the use of etching and takes advantage of the different etch rates of crystallographic planes in the substrate material.

9. A method as claimed in any one of claims 6 to 8 wherein the particles are sized between 0.5nm and 100 microns and will give rise to a wire of dimensions between 0.5nm and 100 microns.

10. A method as claimed in claim 9 wherein the particles are composed of two or more atoms, which may or may not be of the same element.

11. A method as claimed in any one of the preceding claims wherein the accumulation of particles into or against or proximal to, the topographical feature relies upon the diffusion, sliding, bouncing or other movement of the particles across or on the surface of the substrate or any material deposited on the substrate.

12. A method as claimed in any one of the preceding claims wherein the substrate is substantially entirely an insulating or semiconductor material.

13. A method as claimed in claim 12 wherein the etching step removes substantially all of the substrate other than the masked portion thereby leaving a free-standing wire or bridge.

14. A method as claimed in any one of claims 1 to 11 wherein the substrate is an insulating or semiconductor material with one or more surface coatings selected from one or more of a metallic and/or insulating and/or semiconducting material, and wherein one of more of the surface coatings may have been deposited before or after step b) of modifying the substrate surface.

15. A method as claimed in claim 14 wherein the etching step removes substantially entirely all of one or more of the one or more surface coatings other than the masked portion.

16. A method as claimed in 15 wherein the substrate comprises an insulating or semiconductor material coated with one or more metallic and/or semi-conducting layer(s), the metallic and/or semiconducting layer(s) being crystalline, nano- or micro-crystalline, or amorphous.

17. A method as claimed in claim 16 wherein the metallic and/or semiconducting layer(s) are formed by cluster deposition of a plurality of clusters, prior to and having a different identity to, the plurality of particles formed and deposited in steps c) and d).

18. A method as claimed in claim 16 or 17 wherein the metallic and/or semi-conducting layer(s) are homogeneous.

19. A method as claimed in claim 16 or 17 wherein the metallic and/or semi-conducting layer(s) are not homogeneous.

20. A method as claimed in any one of the preceding claims wherein the method may also include treatment of the substrate surface such as by passivation, or adding an insulating layer such as SiOx or SiN, at some point prior to any coating of the substrate with the one or more metallic and/or semiconducting layers.

21. A method as claimed in any one of claims 14 to 20 wherein the method may also include coating of the substrate surface such as by adding an insulating layer such as SiOx or SiN, or different semi-conducting layer, for the purpose of electrical insulation or prevention of oxidation of the metal or semi-conducting layer, at some point subsequent to the substrate being coated with the one or more surface coatings selected from one or more of a metallic and/or insulating and/or semiconducting material.

22. A method as claimed in any one of the preceding claims wherein the method also includes an additional lithography step or steps to provide electrical contact to the pattern.

23. A method as claimed in claim 22 wherein the additional lithography step or steps is/are subsequent to step f).

24. A method as claimed in claims 22 or 23 wherein lithography is used to form two contacts which are separated by a distance smaller than 100 microns.

25. A method as claimed in claim 24 wherein the contacts are separated by a distance less than 1000nm.

26. A method as claimed in any one of the preceding claims wherein the particles are metallic clusters.

27. A method as claimed in any one of the preceding claims wherein the particle/nanoparticle preparation and deposition steps are via inert gas aggregation, or magnetron sputtering and aggregation, or other similar cluster preparation method, and the nanoparticles are atomic clusters made up of a plurality of atoms which may or may not be of the same element.

28. A method as claimed in any one of claims 3 to 26 wherein the semiconductor or insulator of the substrate is selected from silicon, silicon nitride, silicon oxide, aluminium oxide, indium tin oxide, germanium, gallium arsenide or any other III-V semiconductor, quartz, or glass.

29. A method as claimed in any one of claims 16 to 28 wherein the one or more surface coating is/are selected from one or more of aluminium, silicon, platinum, palladium, germanium, silver, gold, copper, iron, nickel or cobalt.

30. A method as claimed in any one or more of claims 5 to 28 wherein the nanoparticles are selected from one or more of bismuth, antimony, aluminium, silicon, platinum, palladium, germanium, silver, gold, copper, iron, nickel or cobalt clusters.

31. A method as claimed in any one of the preceding claims wherein the angle of incidence of the deposition of clusters onto the substrate or the angle of the topographical feature(s) on the substrate is controlled so as to affect the density of particles or their ability to slide, stick or bounce, in or on any part or parts of the substrate.

32. A method as claimed in any one of the preceding claims wherein the kinetic energy of the particles to be deposited on the substrate is controlled by the gas pressures and nozzle diameters of an inert gas aggregation source, or magnetron sputtering and aggregation, or other similar cluster source, and / or associated vacuum system.

33. A method as claimed in claim 32 wherein the conditions are such to encourage diffusion of the nanoparticles on the substrate surface, including one or more of the conditions of temperature, surface smoothness and / or surface type and/or identity.

34. A method as claimed in any one or more of the preceding claims wherein prior to deposition, one or more of the following processes may occur:

- ionisation of particles,

- size selection of particles,
- acceleration and focussing of clusters,
- the step of oxidising or otherwise passivating the surface of the v-groove (or other template) so as to modify the subsequent motion of the incident particles,
- selection of particle and substrate materials and particles' kinetic energy so as to cause the particle to bounce off a part of the substrate (for example the unmodified areas between surface modifications), thereby preventing the adherence of particles in that area of the substrate,
- selection of size of surface modification (e.g. width of V-groove) and so as to control the thickness of the wire formed.

35. A method as claimed in any one or more of the preceding claims wherein the etching step f) results in removal of the substrate material and some or all of any coating materials (if present) in preference to the arrangement of particles.

36. A method as claimed in any one of the preceding claims wherein the etching step f) results in removal of the non-masked coating material in preference to the substrate material.

37. A method as claimed in claim 36 wherein the etching step is a plasma etching process.

38. A method as claimed any one of the preceding claims wherein the method further includes the step of:

    g) removing the etch mask.

39. A method as claimed in any one or more of the preceding claims wherein the substrate contains multiple layers of material, prepared for example by molecular beam epitaxy or metal-organic chemical vapour deposition, such that an anisotropic etching step f) results in formation of a wire in one or more of those layers of material, even in the absence of step g).

40. **A metallic or semi-conducting pattern on the surface of a substrate** prepared substantially according to method claimed in any one of claims 1 to 39.

41. **A method of fabricating a device including or requiring a conduction path between two contacts formed on a substrate surface**, comprising or including the steps of:

   A. preparing a conducting pattern between two contacts according to a method comprising or including the steps of:

      vii. providing a semiconducting or insulating substrate;

      viii. modifying the substrate surface to provide a topographical feature, or identifying a topographical feature on the substrate surface;

      ix. preparing a plurality of clusters;

      x. deposition of a plurality of the clusters on the substrate surface in, or in the general vicinity of, the topographical feature;

      xi. formation of an arrangement of clusters via accumulation (by one means or another), of the clusters, into or against or proximal to, the topographical feature;

      xii. subjecting the substrate and arrangement to an etching process, the arrangement of clusters acting as an etch mask

      wherein either prior to or after step ii. one or more metallic or semiconducting layers are deposited on the substrate surface, such that the etching process removes substantially all of the one or more metallic or semiconducting layers other than the masked portion, and

   wherein the process also includes, at any stage, a step of providing electrical contacts on the substrate so that once etching is complete a conducting pattern exists between the contacts; and

   B. incorporating the contacts and wire into the device.

42. A method as claimed in claim 41 wherein the device includes two or more contacts and the conducting pattern is a conducting wire.

43. A method as claimed in claim 42 wherein the device is a nanoscale device, and the wire is a nanowire.

44. A method as claimed in any of claims 41 to 43 wherein there is an additional step in A of removing the etch mask at some point following the etching process.

45. **A device including or requiring a conduction path between two contacts formed on a substrate surface** prepared substantially according to the method as claimed in any one or claims 41 to 44.

46. **A metallic or semi-conducting pattern on the surface of a substrate** substantially as described herein with reference to any one or more of the Figures and or Examples.